Amendments

Please amend the specification as follows:

At page 8, lines 19-21:

Figure 4 is a simplified formal description of a memory port using an exemplary subset of Verilog in accordance with one embodiment of the present invention.

At page 15, line 25, through page 16, line 3:

Automatic generation of structural descriptions from table-based descriptions is described in U.S. Patent No. 6,148,436, issued on November 14, 2000, entitled "Automatic Generation of Gate-Level Descriptions from Table-Based Descriptions for Electronic Design Automation," by Peter Wohl, assigned to the assignee of the present invention, and is incorporated herein by reference.

Please amend Claim 1 as follows:

1. A method of constructing a structural model of a memory for use in and ATPG (Automatic Test Pattern Generation), said method comprising the steps of:

accessing a simulation model of said memory, from a simulation library stored a computer system memory, wherein said simulation model is described in a behavioral hardware description language;

generating a simplified behavioral model of said memory by re-describing said memory with a predefined subset of said behavioral hardware description language;